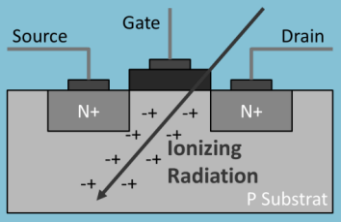
Aging_IP

Monitor for Aging Effects (TID & Stress)



Monitor for Aging Effects (Radiation, Total Ionizing Dose, Temperature, Power and Switching Stress)

Features:

- In Situ Monitoring of aging effects
  - TID (Total Ionizing Dose)
  - Temperature stress
  - Power stress
  - Switching stress
- Inspection of the functionality for Risk Based Maintenance (safety margins)
- Determination of health status and remaining useful life (RUL)
- Customized control interface, easily adaptable for standard interfaces (e.g. JTAG, SPI, I2C)

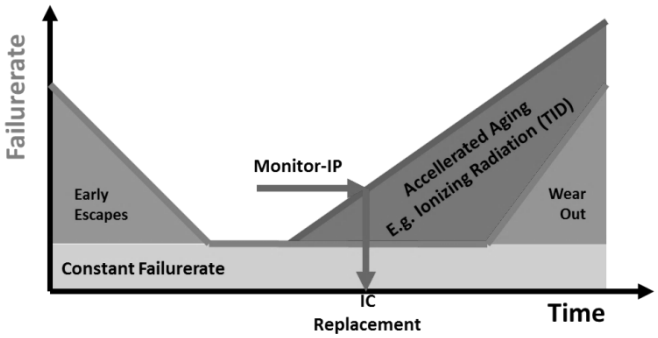


Figure 1 Bathtube Curve

Applications:

- Embedded systems, control systems, signal processing and data storage in high radiation environments (e.g. medical equipment, aviation, aerospace, nuclear power plant)
- Monitor delay degradation due to stress (temperature, switching, power etc.) in long-term system applications
- Out of specification applications (e.g. over temperature)

Targeted Devices:

- Microsemi
  - SmartFusion2
  - Polarfire
- Xilinx
  - Spartan-7
  - Artix-7
  - Virtex-7
- Others supported upon request

Core Deliverables:

- Encrypted VHDL Soft Core
- VHDL Package
- Test Bench
- Application Example
- VHDL Source Code on request

Support:

- Simulation: ModelSim®
- Synthesis: Synplicity®
- Microsemi/Libero®
- Xilinx/Vivado®
- Other tools supported upon request
- Implementation support on request

TESTHAUS AUS ÜBERZEUGUNG

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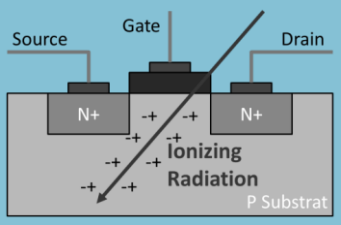

Description:

The configurable Aging IP is designed to detect parameter degradation due to ionizing radiation (nuclear plants, accelerators, medical radiation, cosmic rays, aerospace) or temperature, power and switching stress. It covers the following features:

- Delay Chain Output (DCO)
- DCO counters (DCO0, DCO1)
- Duty cycle deviation
- Min/max delay deviations and flags
- User Interface (ports, registers)

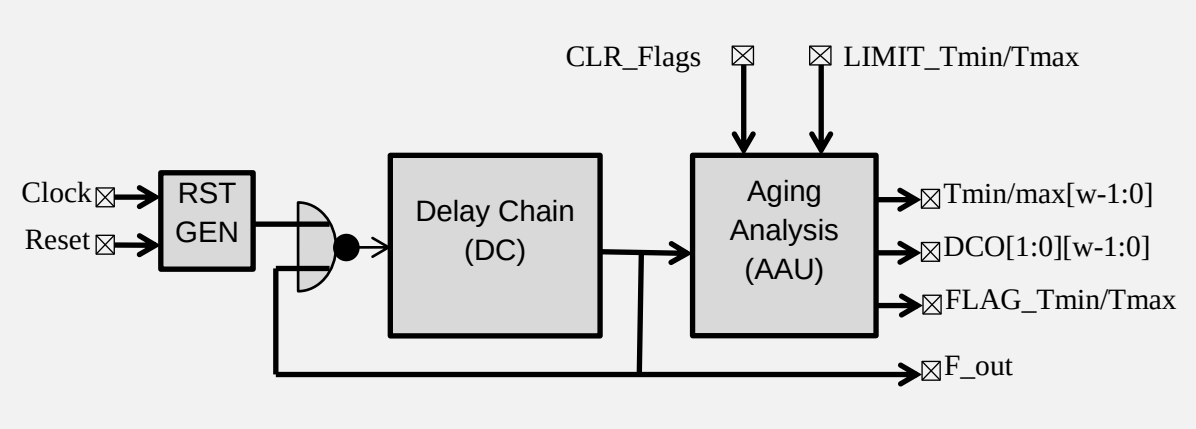

Figure 2 Principle Architecture

The architecture comprises a configurable Delay Chain, a delay analysis block (limits, flags, counters) and a customized user interface for configuration, monitoring and for additional offline analysis.

The aging analysis unit performs timing/frequency measurements and continuous variance analysis and check for min/max limits. The ports of this units can be connected to a User/SW Interface (e.g. SPI) and/or to device IO pins.

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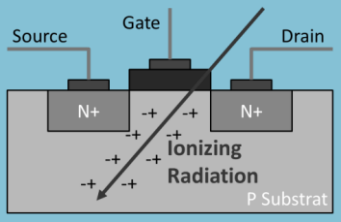

Functional Description

Reset Generator (RSTGEN)

The configurable reset generator converts the asynchronous reset signal into a synchronous reset. It initializes the ring oscillator and resets the flipflops.

Delay Chain (DC)

There is a configurable delay chain implemented consisting of n basic chains. One basic chain consists of m basic cells. A basic cell consists of 10 basic gates (special implementation feature). The non-inverting output of the delay chain is externally available at port F_OUT and is internally fed back to the Delay chain input forming a ring oscillator which is initialized by the RSTGEN block. The n and m numbers are defined in a VHDL package and characterize the specific ring oscillator frequency.

Aging Analysis Unit (AAU)

In situ monitoring of aging effects according TID (Total Ionizing Dose) or electrical and thermal stress by means of inspection of the delay chain and ring oscillator offers Risk Based Maintenance by intelligent timing and frequency measurement and continuous variance analysis. The results are available at the counter outputs DCO[1:0][w-1:0], Tmin/max[w-1:0] and Flag_Tmin/max. The limits for Tmin/max can be set by the two inputs. If these limits are exceeded, the Flag_Tmin/max are set and can be cleared by the input CLR_Flags.

Implementation possibilities

The functionality can be implemented as standalone Diagnosis Device (FPGA) embedded on system boards or embedded as IP-core in system chips (ASIC, SOC, ASSP).

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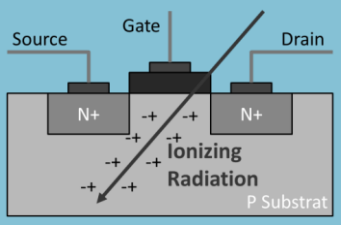

Signal Descriptions

Signal	Direction	Description
clock	input	Clock for the IP block (e.g. 200 MHz)
reset	input	Asynchronous reset signal
clr_flags	input	Clear all flags
limit_tmax[w-1:0]	input	Limit Tmax (raw number of clock cycles)
limit_tmax[w-1:0]	input	Limit Tmax (raw number of clock cycles)
f_out	output	ROSC output for ext. frequency measurements
dco[1:0][w-1:0]	output	DCO counters for high/low period (raw clock cycles)
tmax[w-1:0]	output	Measured max period (raw clock cycles)
tmin[w-1:0]	output	Measured min period (raw clock cycles)
flag_tmax	output	Flag if max limit is exceeded
flag_tmin	output	Flag if min limit is exceeded

Description of Constants (VHDL package)

Generic	Type	Description
c_td	time	average delay per cell
c_clk_period	time	Clock period
c_cells	natural	Number of cells (consisting of 10 basic gates)
c_chains	natural	Number of chains
c_limit_tmax	natural	Limit tmax (raw clock cycles)
c_limit_tmin	natural	Limit tmin (raw clock cycles)
c_rst_clks	natural	Reset length (raw clock cycles)
c_count_width	natural	Width of data/counters
c_sample_size	natural	Sampling for mean value calculation

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