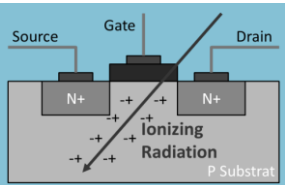

Asymmetrical Degradation and hidden Duty Cycle Distortion of p/n-MOS Transistors due to TID, monitored by a special ROSC Implementation

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Abstract—In CMOS circuits the p- and n-transistors degrade asymmetrical due to ionizing radiation (TID). This phenomenon leads to duty cycle distortion and may result in timing problems, especially in DDR-Designs (double data rate) where both edges of the system clock are active. This effect might be even worse with further technology scaling. Using normal ring-oscillators (ROSC) this dark degradation is hidden due to the inverted nature of the ROSC. With a special implementation of the ROSC this effect can be made visible in ASICs, SOCs and full-custom designs (patent application DE 10 2021 208 363.3 pending).

This was proven with mathematics, digital and real-number modeling (VHDL-RNM) methodology. Thus, a special ROSC might be used in integrated circuits and PCMs (process control modules) on wafer or chip. It can be utilized to determine p- and n-transistor matching (rise/fall timing and drive capability) and as a degradation monitor in ionizing radiation environments like accelerators, space, aerospace, nuclear power plants, and medical radiotherapy.

***Index Terms*—Aging, ASIC, CMOS, DDR-Designs (double data rate), Integrated Circuit, Ionizing Radiation, Real Number Modeling, Process Control Modules, RADSAGA, RedunSys, Ring Oscillator, SOC, Total Ionizing Dose.**

I. Introduction

In ionizing radiation environments there are basically two effects on electronics [1][2][3]: Single event effects (SEE) like transients/upsets (SET/SEU) and total ionizing dose (TID). Single events or soft errors can lead to loss of functionality depending on FIT (Failure in Time) rate and system complexity, e.g. bitflips in configuration memories like SRAM in FPGA or any other configuration Flipflops. TID on the other hand is an accumulated effect which results in performance degradation depending on dose rate and time, e.g. threshold shifts in transistors and increase in delay time and leakage current.

In the research project RedunSys (2008-2010) [4] a first version of a monitoring circuit for these effects with flash-based FPGAs from Actel/Microsemi [5][6][7] in ProAsic3 technology (130nm) was designed. Soft errors could not be detected because of short test times and low system complexity. Therefore, the focus was towards TID measurement. The results are shown in Figure 1. There is a linear degradation of the frequency of the ring oscillator during the first 400Gy (40krad) and an exponential degradation with higher dose rate. Also, a kind of annealing is seen afterwards. After a dose rate above ~1000Gy (100krad) some devices stopped operation due to hardware defects.

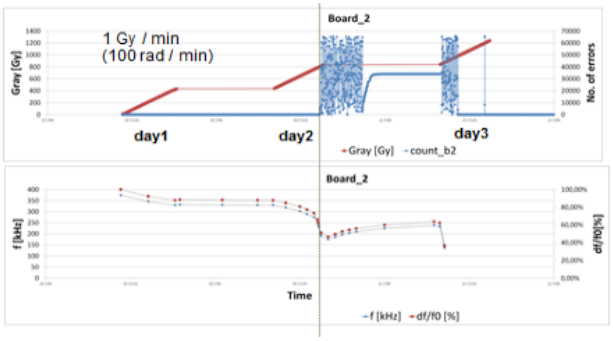

Figure 1: Measurement results in medical radiation environments

In the meantime some work on the topic was done by F. Kastensmidt [9], M. Berg [10], and it was observed that floating gate (FG) transistors within data paths in flash-based FPGAs are main contributors for TID effects in these FPGA technologies [8]. Charge trapping in oxide and STI (shallow trench isolation) regions of the transistors are the main reason for voltage shifts and parasitic leakage currents (A. Michalowska-Forsyth [11]).

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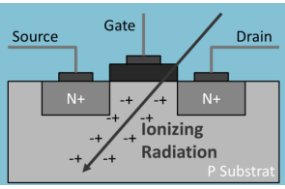

Around 2015, Microsemi issued a new radiation tolerant Flash-FPGA technology RTG4, with decoupled floating gate transistors of data paths (JJ Wang [12]).

In 2020 iSyst GmbH extended the aging topic to normal degradation due to stress (temperature, voltage, frequency) [12][14][15] and did some detailed measurements [16][17][18]. The radiation monitor was optimized with respect to the new stress topics (AgingIP, [19]).

Since 2016 active research for hidden degradation of CMOS transistors is being done at our site which involved investigations and modeling of asymmetrical deviations with digital and VHDL-RNM (real number modeling) simulations [20]. The background of asymmetrical degradation due to TID and the current status of our work is shown in the next chapters.

II. Background

A. *TID & asymmetrical degradation*

In a paper by G. Schlenvogt [21] it was shown, that with decreasing supply voltages and technology feature sizes the p- and n-MOS transistors behave different with increasing dose rates.

Microsemi did extended radiation measurements with delay lines in the RTG4 technology (JJ Wang [12]) but could not find any degradation up to around 200krad (2kGy), but some faster delay paths were observed.

In a recent RADSAGA@Cern [24] presentation (I. Lopes [22]) various ROSCs were used in different FPGA technologies. The degradation was very small and occurred in both directions, faster and slower delay, respectively.

Also, in a paper by G. Borghello [23] it was shown that the p- and n-MOS behave differently in high and ultra-high TID environments, p-MOS is more deteriorated than n-MOS, and n-MOS can even get faster for lower dose rates.

All the work shown are clear indications that asymmetrical degradation is present, but it cannot be monitored by normal ROSC implementations, because its inverted nature masks out the asymmetry and thus the duty cycle distortion is hidden.

B. *TID & transfer curve*

In Figure 2 the transfer curve of a CMOS inverter is shown. The normal one is the green line at ~50% threshold voltage.

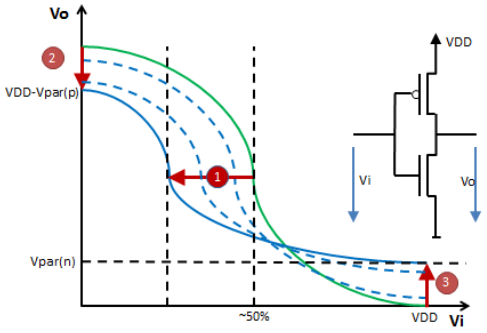

Figure 2: TID & Transfer Curve

Due to TID over time the threshold voltages are modified resulting in a shift of the switching level to the left and slope modification due to resistive changes. Also, voltage degradation at both levels may be infected due to leakage current. All these effects contribute to parameter, delay, leakage and performance degradation of the transistors and gates sensitive to TID. These parameters can be modified for p- and n-MOS transistors independently, thus the asymmetrical deviations can be modeled accordingly.

C. *VHDL-RNM*

An inverter and the complete ROSC can be modeled according to the transfer curve definitions with VHDL-RNM (real number modeling), a kind of switch level modeling and simulation style of RC topologies using a digital VHDL simulator. In Figure 3 the modeling and simulation concept is shown. The generics used, including radiation factors, are shown in Figure 4.

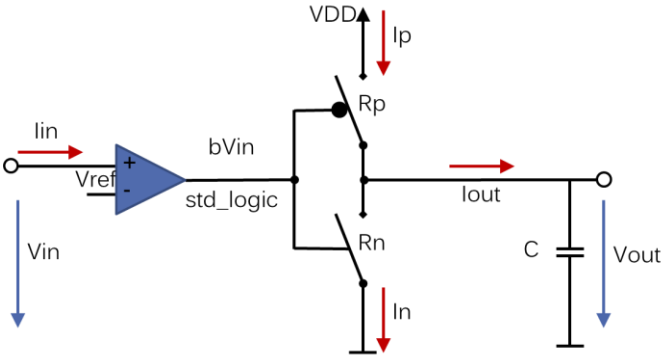

Figure 3 RNM & Switch Level Modeling

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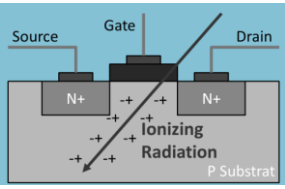


```
entity rosc_inv_rnm is
    generic (
        g_vdd    : real := 5.0;       -- core VDD
        g_sl     : real := 0.50;      -- switch level %
        g_ci     : real := 10.0e-12; -- internal cap (pF, resolution prol
        g_x      : real := 5.0;       -- x factor driver
        g_dt     : real := 0.1e-9;    -- sampling periode
        --
        g_r0     : real := 1000.0;    -- basic resistor value
        g_zp     : real := 1.0;       -- basic pmos factor
        g_zn     : real := 1.0;       -- basic nmos factor
        -- radiation factors
        g_rfsl   : real := 0.0;   -- switching level % (transfer curve)
        g_rfrp   : real := 0.5;   -- resistor p % (delay, slope)
        g_rfrn   : real := 0.0;   -- resistor n % (delay, slope)
        g_rfvdp  : real := 0.0;   -- voltage degradiation p % (leakage i)
        g_rfvdn  : real := 0.0;   -- voltage degradiation n % (leakage i)
        -- ROSC
        g_lro    : integer := 100     -- length of ROSC
    );
```

Figure 4: ROSC_inv_RNM (Generics, with radiation factors)

III. ROSC-IP Algorithm

At our site a special ROSC-implementation was developed to make the asymmetrical degradation and the resulting duty cycle distortion visible. This was proven by mathematics and modeling & simulation with RNM methodology. The principal mathematics is shown in Figure 5. The algorithm and the implementation details for the ROSC-IP are patent application pending [25].

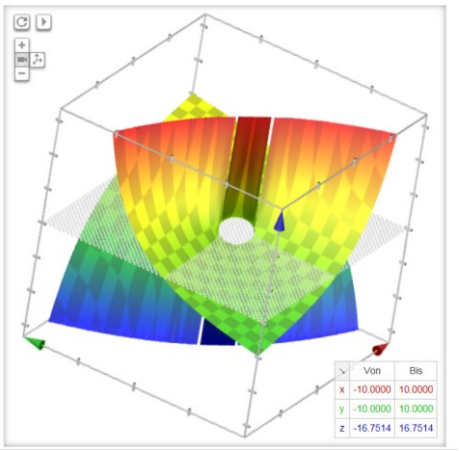

Figure 5: Principle Mathematics of ROSC-IP

In Figure 6 an example of the deviation table is shown. The x variable is a kind of implementation factor. Variable y is a figure for radiation exposure, e.g., deviation of the threshold voltage in percent. The resulting AI (aging index) values are shown in green. For x=1 we get no AI deviations independent of the radiation exposure y. For x=5 and y=50% we get around 31% AI deviation, that is the high to low relation of the resulting ROSC-frequency; thus, the DC (duty cycle) is around 24%.

AI	x									
	1	2	3	4	5	6	7	8	9	10
0	1,000	1,000	1,000	1,000	1,000	1,000	1,000	1,000	1,000	1,000
0,1	1,000	1,032	1,049	1,059	1,066	1,070	1,074	1,077	1,079	1,081
0,2	1,000	1,063	1,095	1,115	1,129	1,139	1,146	1,152	1,157	1,161
0,3	1,000	1,091	1,140	1,170	1,190	1,205	1,217	1,226	1,233	1,239
0,4	1,000	1,118	1,182	1,222	1,250	1,270	1,286	1,298	1,308	1,316
y' 0,5	1,000	1,143	1,222	1,273	1,308	1,333	1,353	1,368	1,381	1,391
0,6	1,000	1,167	1,261	1,321	1,364	1,395	1,419	1,438	1,453	1,466
0,7	1,000	1,189	1,298	1,368	1,418	1,455	1,483	1,505	1,523	1,538
0,8	1,000	1,211	1,333	1,414	1,471	1,513	1,545	1,571	1,593	1,610
0,9	1,000	1,231	1,367	1,458	1,522	1,570	1,607	1,636	1,661	1,681
1	1,000	1,250	1,400	1,500	1,571	1,625	1,667	1,700	1,727	1,750

Figure 6 Aging Index AI=f(x, y)

IV. Simulation Results

A. Digital Simulation

The results of the digital simulation (VHDL-behavioral) are shown in Figure 7. The testbench results are shown in Figure 8.

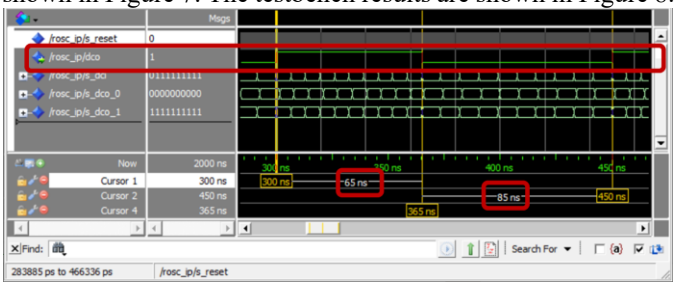

Figure 7 Digital Simulation Results

Item	Result @Time 450 ns	Delta	Delta invers
Htime	65 ns		
Ltime	85 ns		
Alinv=1/AI	1.307692e+00	130,1%	77%
DC=1-DCinv	4.333333e-01	57%	43%
Period T	150 ns		
Frequency f	6.666667e+06 Hz		

Figure 8 Testbench Results

B. VHDL-RNM Simulation

Similarly, in Figure 9 the results of the RNM simulation, with the generics of Figure 4, are shown. The testbench results are shown in Figure 10.

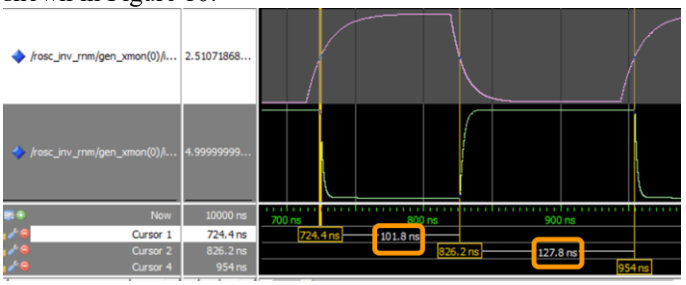

Figure 9 Waveform of RNM Simulation

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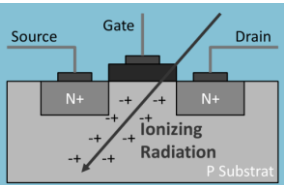

Item@n=10	Result @Time 955400 ps	Delta	Delta invers	Comment
Htime	127 ns			
Ltime	102,5 ns			
AI=1/AIinv	1.245	124,5%	80,3%	Delta due to feedback/resolution
DC=1-DCinv	0.555	55,5%	44,5%	
Period T	229.5 ns			
Frequency f	4.367e+06 Hz			

Figure 10 Testbench Results RNM

In the RNM simulations the feedback inverter of the ROSC was also modeled. The number of buffers was n=10 in these examples. Thus, we get a small deviation of the results compared to the digital and mathematical results. In practice, for better resolution of the AI and frequency measurements, a huge number of buffers are used for the ROSC. Then the deviations due to the feedback inverter are negligible.

V. CONCLUSION & FURTHER WORK

Modeling, simulations and mathematics have shown that asymmetrical TID effects are masked out by the nature of normal ring oscillators due to identical inverters and inverted feedback loop.

The simulation results with a special ROSC implementation show degradation of delay in the same order of percentage like the variance of the applied radiation factors for threshold shifts and resistive degradation.

This was proven by mathematics & RNM-simulations but not by real measurements yet because it cannot be implemented in FPGA technologies, thus ASIC or full-custom designs would be required.

As an associated partner, we are still in close cooperation and discussions with the RADSAGA@Cern research project [24] for further explanations and applications of the ROSC-IP. It could be also of interest for all semiconductor vendors and CMOS technologies (PCM, Monitoring IP etc.) for detecting hidden degradation due to TID, and also for determination of p/n-matching of the CMOS transistors of the library elements.

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