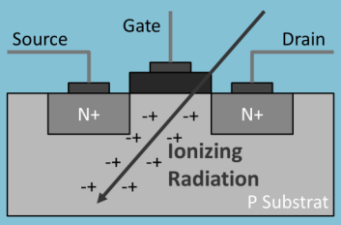
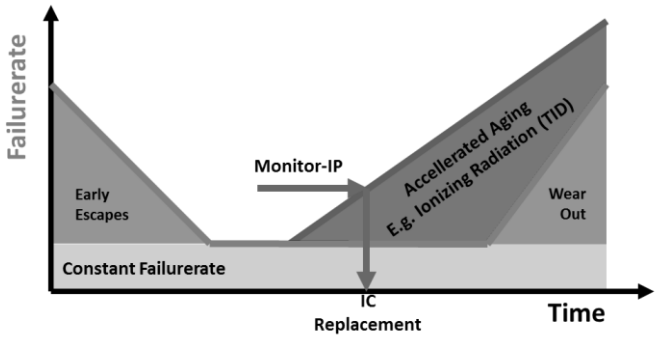
SEU-TID-Core

Detector-IP for Single Event Upsets and Aging



Detector-IP for Single Event Upsets / Aging Effects (Total Ionizing Dose)



Features:

- Error correction according TMR-Voting (Triple Modular Redundancy)
- Error detection to validate SEU (Single Event Upsets) occurrences
- In Situ Monitoring of aging effects according TID (Total Ionizing Dose)
- Inspection of the functionality for Risk Based Maintenance
- Determination of remaining useful life (RUL)
- Customized control interface, easily adapted for standard interface (e.g. JTAG, AHB); conforms to International Standard ISO/IEC 3309 Specification
- Random Fault Insertion (FI) on request

Applications:

- Embedded systems, control systems, signal processing and data store in high radiation environments (e.g. medical equipment, aviation, aerospace, nuclear power plant)
- Robust design and test methodology for use in critical radiation environments for digital integrated circuits (ASIC, FPGA, ASSP)

Targeted Devices:

- Actel/Microsemi Family
- Altera Family
- Xilinx Family

Core Deliverables:

- Encrypted Soft Core
- VHDL Source Code on request
- User Guide
- Test Bench

Synthesis/Simulation Support:

- Synthesis: Synplicity®
- Simulation: ModelSim®
- Other tools supported upon request

Verification Support:

- Test Bench
- Test Vectors
- Reference Models

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TESTHAUS AUS ÜBERZEUGUNG

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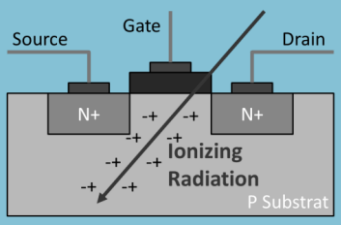
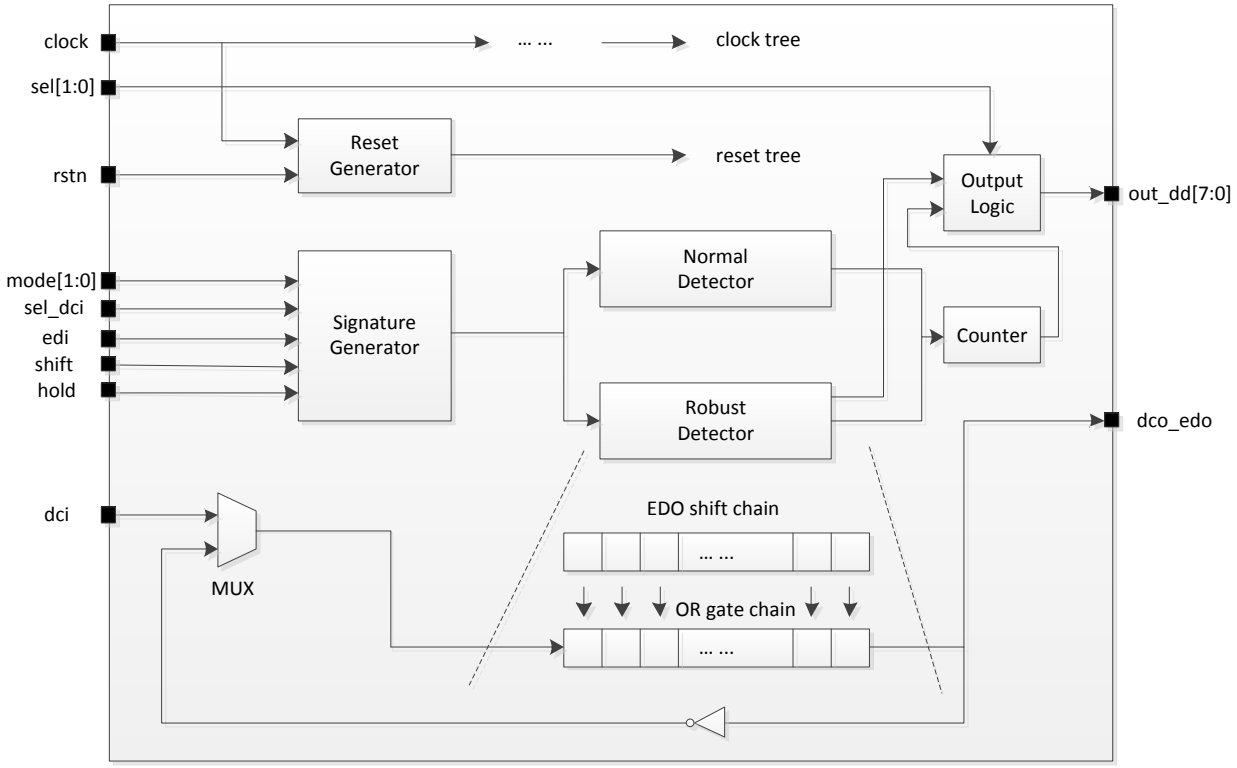


Description:

The configurable IP-Core is designed based on the r-FF methodology to detect radiation effects in high energetic radiation environments. It is able to mitigate soft errors and covers the following features:

- Error Detection (ED)
- Error Location (ED-flag)
- Error Correction (TMR voting)
- Monitoring of aging effects (delay chain)



It comprises a configurable signature generator and a detector array. Error information (values, location, time stamps etc.) is sampled and stored on-chip and can be accessed by a customized interface for offline analysis.

Aging effect monitoring can be done by means of a ring oscillator (frequency measurement and continuous variance analysis) implemented by delay elements in the r-FF structure (delay chain).

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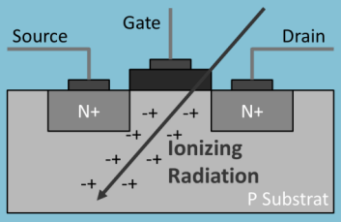

Functional Description

Reset Generator

The reset generator converts the asynchronous reset signal into synchronous reset.

Signature Generator

The signal generator creates the identical testing vectors to for normal detector and robust detector in parallel. It provides a signal pattern to the sensor array. The logic includes two pattern modes: counter (CT) and checker board (CB). During reset the counter is set to zero and the CB-value is set to the initial seed value (e.g. “1010...”). The mode may be used to produce all-ones or all-zeros or any other random pattern for further error analysis.

Normal Detector and Robust Detector

A series of register blocks create a sensor array. There are two functional identical sensors: a normal one (Normal Detector) and a robust one (Robust Detector) built with r-FFs, described above. The registers have the word width X. Each bit of the word is connected in series building a shift register of the length Y thus creating an (X*Y) array to determine the location for the error injection. The error detection inputs and outputs of each register are connected resulting in a daisy chain.

Counter

The counter collects the error information and outputs them to the output logic.

Output Logic

Controlled by the input signal sel[1:0], the output logic block drives the error information or the output from the Robust Detector.

Determination of Aging Effects and remaining useful life (RUL)

In situ monitoring of aging effects according TID (Total Ionizing Dose) by means of inspection of the functionality offers Risk Based Maintenance by intelligent frequency measurement and continuous variance analysis without the need to memorize the initial value of the frequency. Furthermore the realization is independent of temperature and voltage variations of the supply voltage. Thus no calibration is necessary.

Implementation possibilities

The functionality can be implemented as standalone Diagnosis Device (FPGA) embedded on system boards or embedded as IP-core in system chips.

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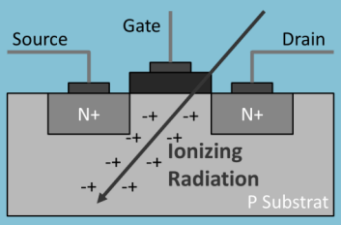

Signal Descriptions

The following signal descriptions define the IO signals.

Signal	Direction	Description
clock	input	Clock for the IP block
rstn	input	Reset signal for the IP block. Low active. Asynchronous reset will be converted into synchronous signal inside the IP block.
sel[1:0]	input	Global select signal:00→ output MSB of the Robust Detector; 01 → LSB of the Counter; 10 → MSB of the counter; 11→ Reserved
mode[1:0]	input	Signature generation controlled signal: 00→ all zero; 01 → all one; 10 → a 01 bit stream like “010101…”; 11→ counter function, the generated signature vector is equal to the output of robust detector plus one
sel_dci	input	Select signal for controlling the MUX to pass dci (when 1) or the inverted feedback of the OR gate chain in the robust detector
dci	input	Data input to the first OR gate in of the OR gate chain in robust detector
edi	input	Error information input to the first r-FF in robust detector
shift	input	Only works when hold = 1: shift the input error information (when shift=1) or the failed information of the current stage to the next stage
hold	input	Capture error information from r-FF (when hold = 0) or shift information to next stage
out_dd[7:0]	output	Data output
dco_eco	output	Error information of the last r-FF in the robust detector

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