# iSPIsim

## Simulation of SPI interfaces

**Hardware:**

Two **SPI interfaces** with one **chip select signal** each.

Up to **20 Mbit/s** bit rate / 20 MHz Operating frequency of the SPI.

**System integration** via **CAN bus** (up to 1 Mbit/s) – optional second CAN interface is available for user-defined applications.

**Software:**

**SPI master functionality**

**SPI slave functionality**

**Full duplex mode**

**Listen-only mode**

**Implementation** of (Application) data from CAN to SPI and vice versa


SPI interface parameters configurable at runtime: **clock polarity**, **phase**, **bit order**, **length of** data communication

Conversion of data from one (e.g. simulation of an A/D converter) to **multiple implementations** of **customer-specific** protocols. All options are feasible.
(Software adaptation is necessary for customer-specific requirements)

Calculation and verification of **CRC checksums** and **parity bits** in the SPI protocol possible

Feedback of errors is issued via CAN bus from the SPI interface.

**Error injection** at data and protocol level (e.g. incorrect data length, incorrect CRC and incorrect parity) - Customizable to customer's requirements.

Simulation of **electrical short circuits** on the SPI supply voltage

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TESTHAUS AUS ÜBERZEUGUNG

**iSyst Intelligente Systeme GmbH** Hugo-Junkers-Str. 9 90411 Nürnberg Tel.: +49 911 37665-0 info@isyst.de www.isyst.de